

REMARKS

Claims 1-13, 16-23 and 25-27 are currently active.

The Examiner has objected to the drawings. It is respectfully submitted that figure 4 covers Claim 26, and reference signs 24 and 26 are found in figure 6.

The Examiner has rejected Claims 7, 8 and 10 under 35 U.S.C. 112, second paragraph. The claims have been amended to obviate this rejection.

The Examiner has rejected Claims 1-5 and 16 as being anticipated by Friedrich. Applicants respectfully traverse this rejection.

Friedrich teaches a circuit for recovering a data signal and regenerating a clock signal can be fully integrated into a chip and has two independent series-mounted regulating steps that can be adjusted optimally in a separate manner. The first regulating step has a wide bandwidth and is optimized for the highest possible jitter tolerance. The second regulating step has a narrow bandwidth and is optimized for the lowest possible jitter transfer. It is respectfully submitted the Examiner is ignoring the specific language that Friedrich uses regarding its teachings and instead is saying that the first regulating step has to do with jitter

and the second regulating step has to do with wander, even though Friedrich is totally silent regarding wander, and instead speaks to regulate wide bandwidth for the highest possible jitter tolerance and the narrow bandwidth for the lowest possible jitter balance transfer.

Applicants' invention of Claim 1 has the limitations of a first filter for removing jitter from the signal and a second filter for moving wander from the signal separate and apart from the first filter. It is respectfully submitted that Friedrich fails to teach or suggest these limitations of Claim 1. Accordingly, Claim 1 is patentable over Friedrich. Claims 2-5 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable. Claim 16 is patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claim 25 as being unpatentable over Jones. Applicants respectfully traverse this rejection. Jones teaches timing synchronization and switchover in a network switch. Claim 25 has the limitation that the backup hardware system uses a first master signal, second master signal and timing distribution signal as a reference signal. Jones fails to teach or suggest this limitation.

Jones teaches that the switch includes two timing modules, one being active while the other is standby. Synchronization of external communications is provided through programmable selection from among plural potential sources of timing at the timing modules.

The active timing module apparatus has a timing master, providing a primary synchronization clock to the system. The standby timing module provides a redundant timing function, configured identically to the active timing module. Both active and standby timing modules have access to the same references, including two external references and two port references. See column 2, lines 37-48. Thus, Jones does not teach a first master signal, second master signal and the timing distribution signal produced by a master hardware system which is used as a reference signal by the backup hardware system. Jones simply teaches to provide a primary synchronization clock to the system and that the active and standby timing modules both have access to the same references. This is in contradistinction to the limitations of Claim 25.


Accordingly, Claim 25 is patentable over Jones.

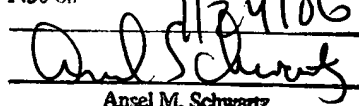
In view of the foregoing remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-13, 16-23 and 25-27, now in this application be allowed.

Respectfully submitted,

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